IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Shunpei Yamazaki
Serial No. : 09/651,310
Filed : August 30, 2000
Title : DISPLAY DEVICE

Art Unit : 2871
Examiner : Kenneth Parker

Commissioner for Patents
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SUPPLEMENTAL REPLY

Supplemental to the reply filed on June 10, 2003, Applicant submits herewith a verified English translation of the priority Japanese application (JP 08-146668, filed May 16, 1996). This submission is believed to overcome the prior art rejection. Accordingly, it is requested that the instant application be allowed.

Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: July 29, 2003

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Docket No.: 07977/151002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Divisional Patent Application of	)
Shunpei YAMAZAKI	) Examiner: K. PARKER
Application No.: 09/651,310	) Art Unit: 2871
Filed: August 30, 2000	)
For: DISPLAY DEVICE	)

VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks

Washington, D.C. 20231

Sir:

I, Noriko Inage, 116-2, Kamioi, Oi-machi, Ashigarakami-gun, Kanagawa-ken 258-0016 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached translation of the Japanese Patent Application No. 08-146668 filed on May 16, 1996; and

that to the best of my knowledge and belief the followings is a true and correct translation of the Japanese Patent Application No. 08-146668 filed on May 16, 1996.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 18th day of June 2003

Name: Noriko Inage

[Name of Document]	Patent Application	
[Reference Number]	P003339-01	
[Filing Date]	May 16, 1996	
[Attention]	Commissioner, Patent Office	
[International Patent Classification]	H01L 21/00	
	G02F 1/133	
[Title of Invention]	Display Device	
[Number of Claims]	5	
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[Indication of Handlings]		
[Method of Payment]	Prepayment	
[Number of Prepayment Note]	002543	
[Payment Amount]	¥ 21,000	
[List of Attachment]		
[Attachment]	Specification	1
[Attachment]	Drawing	1
[Attachment]	Abstract	1

[Name of Document] Specification
[Title of the Invention]

DISPLAY DEVICE

[Scope of Claim]

[Claim 1]

A display device characterized in that the display device comprising:

a structure in which a liquid crystal material is interposed between a pair of substrates; and

a structure in which an active matrix circuit and a peripheral driver circuit are provided on one of said pair of substrate,

wherein said liquid crystal material is sealed with said sealing member,

wherein said peripheral driver circuit is covered with said sealing member, and

wherein said sealing member has a light blocking property.

[Claim 2]

A display device according to claim 1, characterized in that pixels are provided in matrix shape in an active matrix region, and a region overlapping with a pixel electrode of a source line and a drain line functions as a black matrix in said pixels.

[Claim 3]

A display device according to claim 1, characterized in that a electrode or a wiring line which is connected to a source or drain of a thin-film transistor arranged in an active matrix region is formed by a metal film, a semiconductor film or a silicide film, and a light blocking film of said thin-film transistor is formed by utilizing said metal film, said semiconductor film or said silicide film.

[Claim 4]

A display device according to claim 1, characterized in that said pair of substrates is a glass substrate or a quartz substrate.

[Claim 5]

A display device according to claim 1, characterized in that said pair of substrates is bonded each other with said sealing member.

[Detailed Description of the Invention]

[0001]

[Field of Industrial Application]

The present invention disclosed in this specification relates to a structure of an active matrix liquid crystal display device.

[0002]

[Prior Art]

In recent years, active matrix liquid crystal display devices have attracted much attention. In the active matrix liquid crystal display devices, thin-film transistors are provided for each of pixel electrodes that are arranged in matrix form. The thin-film transistors, which are provided for each pixel, have a function of controlling charge entering/exiting from the respective pixel electrodes.

[0003]

The thin-film transistors are formed by using a silicon thin film that is formed on a glass or quartz substrate. Although at present an amorphous silicon film is mainly used as the silicon thin film, it is now expected that in the future a silicon film having crystallinity (referred to as a crystalline silicon film) become the mainstream.

[0004]

The crystalline silicon film is defined as a silicon film whose crystalline structure is more orderly than an amorphous silicon film. Examples of the crystalline silicon film are a polycrystalline silicon film and a microcrystalline silicon film.

[0005]

Forming an active matrix liquid crystal display device by using a crystalline silicon film has characteristics in that not only an active matrix circuit but also peripheral driver circuits can be integrated on the same substrate. This is because the use of a crystalline silicon film allows p-channel thin-film transistors to become suitable for practical use (i.e., allows formation of CMOS transistors) as well as provides thin-film transistors capable of operating at several megahertz (the peripheral driver circuits are required to operate at several megahertz).

[0006]

Active matrix liquid crystal display devices having the above structure are now required to be manufactured at lower costs. To this end, the structure needs to be

simplified.

[0007]

On the other hand, it is also required that the overall size of the device be made smaller. This requirement is arised when a liquid crystal display device is used as a display of portable video cameras and portable business equipment, and further of various types of information terminal equipment. That is, the portable video cameras and the portable business equipment are required to be reduced in size, and accordingly the display itself is also required to be made as small (or light) as possible.

[0008]

[Problem to be Solved by the Invention]

An object of the present invention is to simplify the structure of an active matrix liquid crystal display device, and to miniaturize its overall size.

[0009]

[Means for Solving the Problem]

According to the present invention, there is provided a display device characterized in that the display device comprising: a structure in which a liquid crystal material is interposed between and held by a pair of substrates; and a structure in which an active matrix circuit and a peripheral driver circuit are provided on one of said pair of substrates; wherein said liquid crystal material is sealed by a sealing member, wherein said peripheral driver circuit is covered by said sealing member, and wherein said sealing member has a light blocking property.

[0010]

In the above structure, it is characterized in that the active matrix region may have pixels that are arranged in matrix form, and regions in each of the pixels where source lines and drain lines overlapped with a pixel electrode may serve as a black matrix.

[0011]

In the above structure, it is characterized in that an electrode or a wiring line connected to a source or drain of a thin-film transistor provided in the active matrix region is composed of a metal film or a semiconductor film, or a silicide film, and a light blocking film for the thin-film transistor is formed by using the one of the metal film, the semiconductor film, and the silicide film.

[0012]

In the above structure, it is characterized in that the pair of substrates is a glass substrate or a quartz substrate.

[0013]

In the above structure, it is characterized in that the pair of substrates is bonded to each other with the sealing member.

[0014]

[Embodiment Mode of the Invention]

As shown in Fig. 6, it is characterized in that the display device comprising: a structure in which a liquid crystal material 439 is interposed between and held by a pair of substrates 434 and 401 and sealed by a sealing member 437; and a structure in which an active matrix circuit and a peripheral driver circuit is provided on the substrate 401 of the pair of substrates, wherein the peripheral driver circuit is covered with the sealing member 437, and wherein the sealing member has a light blocking property.

[0015]

That is, the peripheral driver circuit is shielded from light by the sealing member 437.

[0016]

[Embodiments]

[Embodiment 1]

Fig. 1 outlines an active matrix liquid crystal panel (liquid crystal display device) 101 which incorporates peripheral driver circuits as integral components.

[0017]

In Fig. 1, reference numeral 104 denotes an active matrix circuit, in which pixels are arranged in matrix form.

[0018]

Each pixel is constructed as shown in reference numeral 107 of Fig. 1. That is, each pixel illustrated by reference numeral 107 is provided with a thin-film transistor 108 to which a gate line 112 and a source line 111 are connected.

[0019]

Gate lines and source lines are arranged in lattice form in the active matrix region,

and pixels are provided in the vicinity of the respective intersections of those lines.

[0020]

A pixel electrode is connected to the drain of the thin-film transistor 108, and an electric field is applied to a liquid crystal 109 from the pixel electrode. An auxiliary capacitor 110 is connected in parallel to the liquid crystal 109, to compensate for its charge holding characteristic.

[0021]

Reference numerals 102 and 103 are peripheral driver circuits. These peripheral driver circuits are composed by using shift resisters. Of course, other structures can be used as these peripheral circuits. More specifically, reference numerals 102 and 103 in Fig. 1 denote a source driver circuit and a gate driver circuit, respectively.

[0022]

Fig. 2 shows an example of the structure of the peripheral driver circuits. Further, in Fig. 2, an example of a gate driver circuits for supplying drive signals to the gate lines.

[0023]

In Fig. 2, reference numeral 201 denotes a shift resister circuit. Each circuit consisting the shift resister 201 is composed by a clocked inverter or an inverter as show in Figs. 3A and 3B.

[0024]

Further, in Fig. 2, reference numeral 202 denotes a NAND circuit; 203, a level shifter; 204, a buffer circuit for providing a necessary driving ability; and 205, an active matrix circuit.

[0025]

Returning to Fig. 1, reference numeral 106 denotes an inverter circuit as the most fundamental circuit that constitutes the peripheral driver circuits.

[0026]

In Fig. 1, reference numeral 105 denotes an area in which a resin member for sealing exists. This sealing member serves to bond together a pair of glass substrates (or quartz substrates) that are not apparent from Fig. 1 as well as to prevent an inside liquid crystal from leaking out.

[0027]

The peripheral driver circuits 102 and 103 are disposed in the area 105 where the sealing member exists. With this structure, the area other than the active matrix circuit (which determines the screen size) can be minimized.

[0028]

Since the active matrix region determines the screen size, it cannot readily be made smaller. (The screen should be as large as possible.)

[0029]

Therefore, the structure of Fig. 1 is effective in reducing the size of the entire device.

[0030]

Figs. 4A to 4D show a manufacturing process of an active matrix liquid crystal display device (a manufacturing process of a structure of a TFT substrate side) as shown in Fig. 1. More specifically, a manufacturing process of a CMOS structure to be provided in the peripheral driver circuits denoted by 102 or 103 shown in Fig. 1 and a p-channel thin-film transistor to be provided in the active matrix region.

[0031]

The step shown in Fig. 4A will be described first. First, a base film not shown in the figure is formed on a glass substrate 401. In this embodiment, a silicon oxide film is used as the base film. The silicon oxide film is formed by a sputtering method (or plasma CVD). The film thickness of the base film is se to 3,000 Å.

[0032]

Then, a silicon film which becomes a starting film for constituting an active layer of a thin-film transistor in the latter step is formed in the following manner. First, a 500Å thick amorphous silicon film is formed by low-pressure thermal CVD. Plasma CVD or sputtering may be used instead of low pressure thermal CVD for the formation of the amorphous silicon film.

[0033]

The amorphous silicon film, which is not shown in the figure, is then crystallized by irradiating with laser light. More specifically, the amorphous silicon film is crystallized, i.e., converted into a crystalline silicon film by irradiating with KrF excimer laser light (wavelength: 248 nm). Laser light is shaped into a linear beam, and then applied to the film while scanning it. This enables processing of a large-sized substrate.

[0034]

As still another method of forming the crystalline silicon film, a heat treatment or a combination of laser light and the heat treatment can be used.

[0035]

The resulting crystalline silicon film is patterned. By the patterning, active layers 402, 403 and 404 of the thin-film transistors can be obtained. (Fig. 4A)

[0036]

Here, the active layers 402 and 403 become active layers of a p-channel thin-film transistor and an n-channel thin-film transistor that constitute a CMOS circuit to be disposed in the peripheral driver circuit. Note that the p-channel thin-film transistors are denoted by PTFT whereas the n-channel thin-film transistors are denoted by NTFT in the figure.

[0037]

Further, the active layer 404 becomes an active layer of a p-channel thin-film transistor provided in the active matrix circuit. The p-channel thin-film transistor is provided for each pixel.

[0038]

After the active layers denoted by 402, 403, and 404 are formed, a silicon oxide film which functions as a gate insulating film is formed. Here, the silicon oxide film is formed with a film thickness of 1,000Å by the plasma CVD. Thus, the state shown in Fig. 4A is obtained

[0039]

Subsequently, an aluminum film that becomes a sating film for constituting gate electrodes (and gate lines) is formed by the sputtering. Here, the aluminum film is formed with a film thickness of 4,000Å.

[0040]

Scandium is added to the aluminum film at 0.1 wt% to prevent hillocks and whiskers from occurring in a later heating step or laser light irradiation step.

[0041]

Hillocks and whiskers are horn or needle-like protrusions formed by abnormal growth of aluminum. Note that yttrium may be used instead of scandium.

[0042]

Instead of the aluminum film, tantalum etc. can be used. In more general terms, materials capable of being anodized may be used. Metal materials and silicide materials may be used. Further, semiconductor materials doped with an impurity for imparting conductivity at a high concentration may also be used.

[0043]

After the formation of the aluminum film not shown in the figure, an anodic oxide film not shown in the figure is formed with a film thickness of 100 Å by anodization. In this step, an ethylene glycol solution containing tartaric acid at 3% is used as an electrolyte.

In this solution, the aluminum film is used as the anode and platinum is used as the cathode.

[0044]

A resulting anodic oxide film is a dense film in this step. The thickness of the anodic oxide film can be controlled by the application voltage.

[0045]

Next, a resist mask that is not shown in the figure is formed. Then, the aluminum film is patterned to form aluminum patterns that become gate electrodes denoted by 406, 407 and 408. These aluminum patterns are referred to as a first-layer wiring.

[0046]

In the active matrix region, the gate electrode 408 is so formed as to extend from a gate line (for example, denoted by reference numeral 112 in Fig. 1).

[0047]

Thereafter, anodization is again performed with the aluminum patterns 406 to 408, which will become gate electrodes, as the anodes. The conditions other than the thickness control condition are set the same as those in the previous anodization.

[0048]

In this step, dense anodic oxide films 409, 410 and 411 are formed with a film thickness of 1,200Å.

[0049]

These anodic oxide films have effects of preventing short-circuiting between the

gate electrodes (gate lines) and other wiring lines through an interlayer insulating film and preventing occurrence of hillocks and whiskers.

[0050]

After the formation of the gate electrodes, source and drain regions of the respective thin-film transistors are formed by injecting impurity ions. First, B ions are injected while the region to become n-channel thin-film transistors (NTFTs) is masked with a resist.

[0051]

P ions are then injected while the regions to become p-channel thin-film transistors (PTFTs) are masked with a resist.

[0052]

By injecting the B ions, the regions 412, 414, 418 and 420 become P-type impurity regions. In addition, the regions 412 and 718 are source regions whereas the regions 414 and 420 are drain regions.

[0053]

Further reference numerals 413 and 419 are defined as channel-forming regions of the PTFTs.

[0054]

On the other hand, by injecting the P ions, regions denoted by 415 and 417 become n-type impurity regions. Further, a region denoted by 416 is defined as a channel-forming region of the NTFT.

[0055]

After the impurity ions implantation, laser light irradiation is performed to activate the injected impurity elements and anneal damage that is caused by ion impact. KrF excimer laser light is used here.

[0056]

Subsequently, a silicon nitride film is formed as a first interlayer insulating film 421. The silicon nitride film is formed with a film thickness of 4,000Å by plasma CVD. In addition to the silicon nitride film, a silicon oxide film can be used as the first interlayer insulating film. Furthermore, a lamination film of a silicon nitride film and a silicon oxide film can be used.

[0057]

After the formation of the first interlayer insulating film 421, contact holes are formed. Source electrodes 422 and 424 of the thin-film transistors of the CMOS circuit to be disposed in the peripheral driver circuit are shown in the figure. Further, a source electrode 425 of the thin-film transistor to be disposed in the active matrix circuit is also shown in the figure.

[0058]

The source electrodes 423, 424 are so formed as to extend from source lines in the peripheral driver circuit. Further, the source electrode 425 is so formed as to extend from source lines which is arranged in a lattice form together with gate lines 112 as shown in reference numeral 111 of Fig. 1.

[0059]

A drain electrode 423 is common to the PTFTs and NTFTs, and extends from a drain line that wired to have a necessary pattern. A drain electrode 426 will be brought into contact with a pixel electrode.

[0060]

Each of the above electrodes is a multi-layer film in which a titanium film, an aluminum film and titanium film are laminated. More specifically, a 3,000Å-thick aluminum film is interposed between 500Å-thick titanium films. These films are formed by sputtering.

[0061]

The above electrodes and wiring lines are referred to as second-layer wiring lines.

[0062]

Thus, the state shown in Fig. 4C is obtained. Next, a second interlayer insulating film 427 is formed. A 2,000Å-thick silicon nitride film formed by plasma CVD is used as the second interlayer insulating film, here. In addition, a silicon oxide film and other lamination films may also be used as the interlayer insulating film 427.

[0063]

Next, contact holes are formed, and electrodes denoted by reference numerals 428 and 430 are formed. At the same time, a pattern 429 to serve as a light blocking layer for the thin-film transistor is formed. The thickness of these electrodes and pattern is

set at 2,000Å. These electrodes and pattern are referred to as third-layer wiring lines.

[0064]

Here, a lamination film in which a titanium film, an aluminum film and a titanium film are laminated is used. In addition, various kinds of silicide materials as well as semiconductor materials may be used. Note that, they are required to have optical characteristics which functions as the light blocking layer.

[0065]

Thus, the state shown in Fig. 4D is obtained.

[0066]

Thereafter, as shown in Fig. 5A, a third interlayer insulating film 431 is formed with a film thickness of 2,000Å. As in the above cases, the third interlayer insulating film 431 is a silicon nitride film formed by plasma CVD. Alternatively, the third interlayer insulating film 431 may be made from resin materials.

[0067]

After a contact hole is formed, a pixel electrode 432 is made from an ITO film. Thus, the state shown in Fig. 5A is obtained.

[0068]

Subsequently, a rubbing film 433 for orientating liquid crystals is formed by spin coating. A polyimide film is used as the rubbing film here. Then, known orientation processing is performed. (Fig. 5B)

[0069]

Next, a substrate to be opposed the substrate (denoted by 401 in Fig. 4A) on which the thin-film transistors are arranged is prepared. (Fig. 6)

[0070]

This substrate is configured such that a base film not shown in the figure is formed on a glass substrate 434 that is the same as the substrate 401, an opposed electrode 435 is formed thereon, and an orientation film 436 is formed thereon. Note that the opposed electrode is composed of an ITO.

[0071]

As shown in Fig. 6, the substrates 434 and 401 are bonded together. The distance between the substrates is retained by a spacer 438. The bonding is effected by a sealing

member 437. A liquid crystal material 439 is injected into the inside space of the sealing member 437.

[0072]

The sealing member 437 has the following multiple functions:

- bonding together the substrates 434 and 401;
- sealing the liquid crystal material 439; and
- shielding the peripheral driver circuits from light.

[0073]

The sealing member 437 is made from a resin material containing a pigment for light blocking. For this purpose, various types of resin materials having a light blocking function may be used.

[0074]

Note that, the light blocking function as used herein indicates a function of providing such light blocking property as to prevent operational error and unstable operation of the thin-film transistors constituting the peripheral driver circuits.

[0075]

Therefore, the degree of light blocking depends on the intensity of light that is irradiated to the liquid crystal panel as well as the operation speed and the mode of operation required for the peripheral driver circuits.

[0076]

In the structure shown in this embodiment, the peripheral driver circuits are sealed with the sealing member having the light blocking function. By applying this structure, area other than the region that functions as the screen can be minimized as much as possible.

[0077]

Further, the active matrix region has a structure in which a BM (black matrix) is not provided. (This structure is described later.)

[0078]

Instead of the structure in which the black matrix is not provided, the thin-film transistors of the active matrix circuits have a structure in which a light blocking film 429 (see Fig. 4D) that is simultaneously formed with the third-layer wiring lines is

disposed.

[0079]

In this embodiment, instead of providing the BM (black matrix), the source lines and the gate lines are partly overlapped with the pixel electrodes, and the partly overlapped portions are used as a BM (black matrix).

[0080]

That is, as shown in a top view of Fig. 7, the pixel electrode 430, the source line 111 and the gate lines 112 are provided so as to overlap each other. The overlapping portions functions as the BM (black matrix).

[0081]

Incidentally, same reference numerals of Fig. 7 as in Figs. 1 and 4 through 6 indicate the same parts.

[0082]

In Fig. 7, reference numerals 701 and 702 denote contacts; 404, the active layer of the thin-film transistors; 408, the gate electrode; and 429, the light blocking film shown in Fig. 4D. By using the light blocking film, the thin-film transistors of the active matrix region is not irradiated with light.

[0083]

Although, the present embodiment shows the structure in which the p-channel thin-film transistors are provided in the active matrix circuit, n-channel thin-film transistors may be arranged therein.

[0084]

[Embodiment 2]

Figs 8A to 8E, 9A to 9D, and 10A to 10B show a manufacturing process according to this embodiment. This embodiment shows a structure in which an n-channel thin-film transistor and a p-channel thin-film transistor are formed in a peripheral driver circuit and p-channel thin-film transistors are formed in an active matrix circuit.

[0085]

In particular, this embodiment relates to a structure in which low-concentration impurity regions are formed in the n-channel thin-film transistors and high-concentration impurity regions are formed between the source/drain regions and a

channel-forming region of the p-channel thin-film transistors.

[0086]

This structure can suppress the deterioration in the characteristics of the n-channel thin-film transistors in the peripheral driver circuit. Further, in the active matrix circuit, a variation in on-current value can be reduced.

[0087]

The manufacturing process will be described hereinafter. First, a base film, which not shown in the figures, is formed on a glass substrate 801 as shown in Fig. 8A. A silicon oxide film is used as the base film.

[0088]

Next, an amorphous silicon film, which is not shown in the figure, is formed on the base film with a film thickness of 500Å by plasma CVD. Further, the amorphous silicon film is crystallized by irradiating it laser light, thereby obtaining a crystalline silicon film.

[0089]

The crystalline silicon film is patterned to form an active layer of the thin-film transistors which are denoted by reference numeral 802 and 803. Here, reference numeral 802 denotes an active layer of an n-channel thin-film transistor which is formed in the peripheral driver circuit. Reference numeral 803 denotes an active layer of a p-channel thin-film transistor which is formed in the active matrix circuit.

[0090]

Thereafter, a silicon oxide film is formed as a gate insulating film 804 with a film thickness of 1,000Å by plasma CVD. Thus, the state shown in Fig. 8A is obtained.

[0091]

After the state shown in Fig. 8A is obtained, an aluminum film not shown in the figure is formed to form a gate electrode (and a gate line) with a film thickness of 4,000Å by sputtering. The aluminum film contains scandium at 0.1 wt%.

[0092]

Then, a dense anodic oxide film, which is not sown in the figure, is formed with a film thickness of 100Å. This anodization is performed by using an ethylene glycol solution containing tartaric acid at 3% as an electrolyte solution. Note that, this solution is neutralized with aqueous ammonia.

[0093]

This anodic oxide film has a function for improving the adhesiveness of resist masks that are formed later.

[0094]

Next, the aluminum film is patterned by utilizing resist masks 805 and 806. During this process, aluminum patterns, which become a base of gate electrodes denoted by reference numerals 807 and 808, are formed. Thus, the state shown in Fig. 8B is obtained.

[0095]

In this state, anodization is performed with the aluminum patterns 807 and 808 used as the anodes. In this step, porous anodic oxide members (the term "film" is not appropriate) denoted by reference numerals 811 and 812 are formed. The growth distance of the anodic oxide members is set at 5,000Å.

[0096]

The anodization is performed by using an aqueous solution containing oxalic acid at 3% as an electrolyte.

[0097]

In this step, because of the existence of the resist masks 805 and 806, anodization proceeds selectively on the side faces of the aluminum patterns 807 and 808. That is, the resist masks 805 and 806 prevents the electrolyte from contacting with the top faces of the aluminum patterns 807 and 808. Here, reference numerals 809 and 810 will become gate electrodes in the latter step.

[0098]

Next, the resist masks 805 and 806 are removed. And then, an anodic oxide film that has a dense film is formed. This anodization is performed by using an ethylene glycol solution containing tartaric acid at 3% as an electrolyte solution. Incidentally, this solution is neutralized with aqueous ammonia.

[0099]

In this step, the electrolyte solution penetrates into the porous anodic oxide films 811 and 812. Therefore, anodic oxide films having dense film quality are formed as shown in reference numerals 813 and 814.

[0100]

In this step, the gate electrodes 809 and 810 are defined. The surfaces of these gate electrodes are covered with the anodic oxide films 813 and 814 that have a dense film quality. Further, these gate electrodes and wiring lines extending therefrom constitute first-layer wiring lines. Thus, the state shown in Fig. 8D is obtained.

[0101]

Subsequently, P (phosphorus) ions are injected from above the entire surface. To form source and drain regions, P ions are injected at a relatively high concentration. (Fig. 8E)

[0102]

In this step, the P ions are injected in regions 815, 817, 818, 820, respectively. Further, the P ions are not injected in regions 816 and 819

[0103]

Then, the porous anodic oxide films 811 and 812 are removed to obtain the state shown in Fig. 9A. In this state, the P ions are again injected. In this step, the injection of the P ions are conducted at a lower dosage than in the doping condition shown in Fig. 8E.

[0104]

As result, regions denoted by 821, 822, 823, and 824 are formed as low concentration impurity regions. Then, a channel-forming region 80 of an n-channel thin film transistor is defined. (Fig. 9A)

[0105]

Then, after the region to become the n-channel thin-film transistor is covered with a resist mask 825, B (boron) ions are injected. This step is performed under such conditions that regions 81 and 85 become source and drain regions of the p-channel thin-film transistor.

[0106]

As result the regions denoted by 81 and 85 become source/drain regions. Further, regions denoted by 82 and 84 are formed as regions that exhibit stronger P-type conductivity.

[0107]

This is because the P elements concentration contained in the regions 82 and 84 is lower than that of the regions 81 and 85.

[0108]

That is. B elements for neutralizing the P elements are more required for the regions 81 and 85. As result, there is a state in which the regions 82 and 84 exhibit stronger P-type conductivity than the regions 81 and 85.

[0109]

After the completion of the impurity ion implantation, the resist mask 825 is removed. Then, laser light irradiation is performed to activate the injected impurities and anneal damage in the semiconductor film that is caused by ion impact.

[0110]

Subsequently, a first interlayer insulating film 826 is formed. After contact holes are formed, second-layer wiring lines (electrodes) 827 to 830 are formed. (Fig. 9C)

[0111]

Then, a second interlayer insulating film 930 is formed. After contact holes are formed, third-layer wiring lines (electrodes) 831 and 833 are formed. At the same time, a light blocking film 832 for shielding the thin-film transistor arranged in the active matrix circuit from light is formed. (Fig. 9D)

[0112]

Further, a third interlayer insulating film 86 is formed. After a contact hole is formed, an pixel electrode 834 is formed by using an ITO. A rubbing film 835 is then formed. (Fig. 10A)

[0113]

Thereafter, an opposed substrate 836 is prepared and bonded to the TFT side substrate. An opposed electrode 837 and a rubbing film 838 are formed on the opposed substrate 836

[0114]

Thus, a liquid crystal cell shown in Fig. 10B is completed. In Fig. 10B, reference numeral 839 denotes a resin member having a light blocking function. This resin member includes function of sealing a liquid crystal, bonding the substrates, and other functions. In addition, reference numeral 841 is a spacer for determining the cell gap.

[0115]

[Embodiment 3]

This embodiment is characterized in that the active matrix region is provided, in an equivalent sense, with a series connection of a plurality of thin-film transistors rather than a single thin-film transistor.

[0116]

In this structure, since a divided, small voltage is applied to each thin-film transistor, leak current in an off-state can be reduced.

[0117]

Further deteriorations can be suppressed. Especially, when n-channel thin-film transistors are used, the deteriorations can be remarkably suppressed

[0118]

[Effect of the Invention]

According to the invention as disclosed in this specification, the structure of the active matrix liquid crystal display device can be simplified and whole size of the active matrix liquid crystal display device can be miniaturized.

[0119]

That is, the peripheral driver circuits are disposed in the area where the sealing member exists, the sealing member is used as the light blocking member for the peripheral driver circuits, and no black matrix is disposed in the active matrix region. With this structure, the invention simplifies the structure of the active matrix liquid crystal display device as well as reduce its whole size.

[Brief Description of the Drawings]

[Fig. 1] Fig. 1 is a diagram showing an outline of an active matrix liquid crystal display device.

[Fig. 2] Fig. 2 is a diagram showing an outline of a circuit structure of an active matrix liquid crystal display device.

[Fig. 3] Fig. 3 is a diagram showing a circuit structure.

[Fig. 4] Fig. 4 is a diagram showing a manufacturing process of thin-film transistors that constitute an active matrix liquid crystal display device.

[Fig. 5] Fig. 5 is a diagram showing a manufacturing method of thin-film transistors that constitute an active matrix liquid crystal display device.

[Fig. 6] Fig. 5 is a diagram showing a manufacturing method of thin-film transistors that constitute an active matrix liquid crystal display device. (A diagram showing a cross sectional of a liquid crystal panel.)

[Fig. 7] Fig. 7 is a diagram showing a part of an active matrix region.

[Fig. 8] Fig. 8 is a diagram showing a manufacturing method of thin-film transistors that constitute an active matrix liquid crystal display device.

[Fig. 9] Fig. 9 is a diagram showing a manufacturing method of thin-film transistors that constitute an active matrix liquid crystal display device.

[Fig. 10] Fig. 10 is a diagram showing a manufacturing method of thin-film transistors that constituting an active matrix liquid crystal display device. (A diagram showing a cross sectional of a liquid crystal panel.)

[Description of Reference Symbols]

101 LIQUID CRYSTAL PANEL

102 PERIPHERAL DRIVER CIRCUIT (SOURCE DRIVER CIRCUIT)

103 PERIPHERAL DRIVER CIRCUIT (GATE DRIVER CIRCUIT)

104 ACTIVE MATRIX CIRCUIT

105 REGION IN WHICH SEALING MEMBER EXIST

106 CMOS CIRCUIT CONSTITUTING PERIPHERAL DRIVER CIRCUIT

107 STRUCTURE OF PIXEL CONSTITUTING ACTIVE MATRIX CIRCUIT

108 THIN FILM TRANSISTOR

109 LIQUID CRYSTAL MATERIAL

110 AUXILIARY CAPACITOR

111 SOURCE LINE

112 GATE LINE

201 SHIFT RESISTER CIRCUIT

202 NAND CIRCUIT

203 LEVEL SHIFTER

204 BUFFER CIRCUIT

205 ACTIVE MATRIX CIRCUIT

401 GLASS SUBSTRATE (OR QUARTZ SUBSTRATE)

402, 403 ACTIVE LAYER

404 ACTIVE LAYER

405 GATE INSULATING FILM (SILICON OXIDE FILM)

406, 407 GATE ELECTRODE

408 GATE ELECTRODE

409. 410 ANODIC OXIDE FILM

411 ANODIC OXIDE FILM

412 SOURCE REGION

413 CHANNEL-FORMING REGION

414 DRAIN REGION

415 DRAIN REGION

416 CHANNEL-FORMING REGION

417 SOURCE REGION

418 SOURCE REGION

419 CHANNEL-FORMING REGION

420 DRAIN REGION

421 FIRST INTERLAYER INSULATING FILM

422 SOURCE ELECTRODE (SOURCE LINE)

423 DRAIN ELECTRODE (DRAIN LINE)

424 SOURCE ELECTRODE (SOURCE LINE)

425 SOURCE ELECTRODE (SOURCE LINE)

426 DRAIN ELECTRODE (DRAIN LINE)

427 FIRST INTERLAYER INSULATING FILM

428 DRAIN ELECTRODE (DRAIN LINE)

429 LIGHT BLOCKING FILM

430 DRAIN ELECTRODE (DRAIN LINE)

431 THIRD INTERLAYER INSULATING FILM

432 PIXEL ELECTRODE (ITO ELECTRODE)

433 ORIENTATION FILM

434 OPPOSED ELECTRODE (GLASS SUBSTRATE)

435 OPPOSED ELECTRODE (ITO ELECTRODE)

436 ORIENTATION FILM

437 SEALING MEMBER (INCLUDING LIGHT BLOCKING FUNCTION)

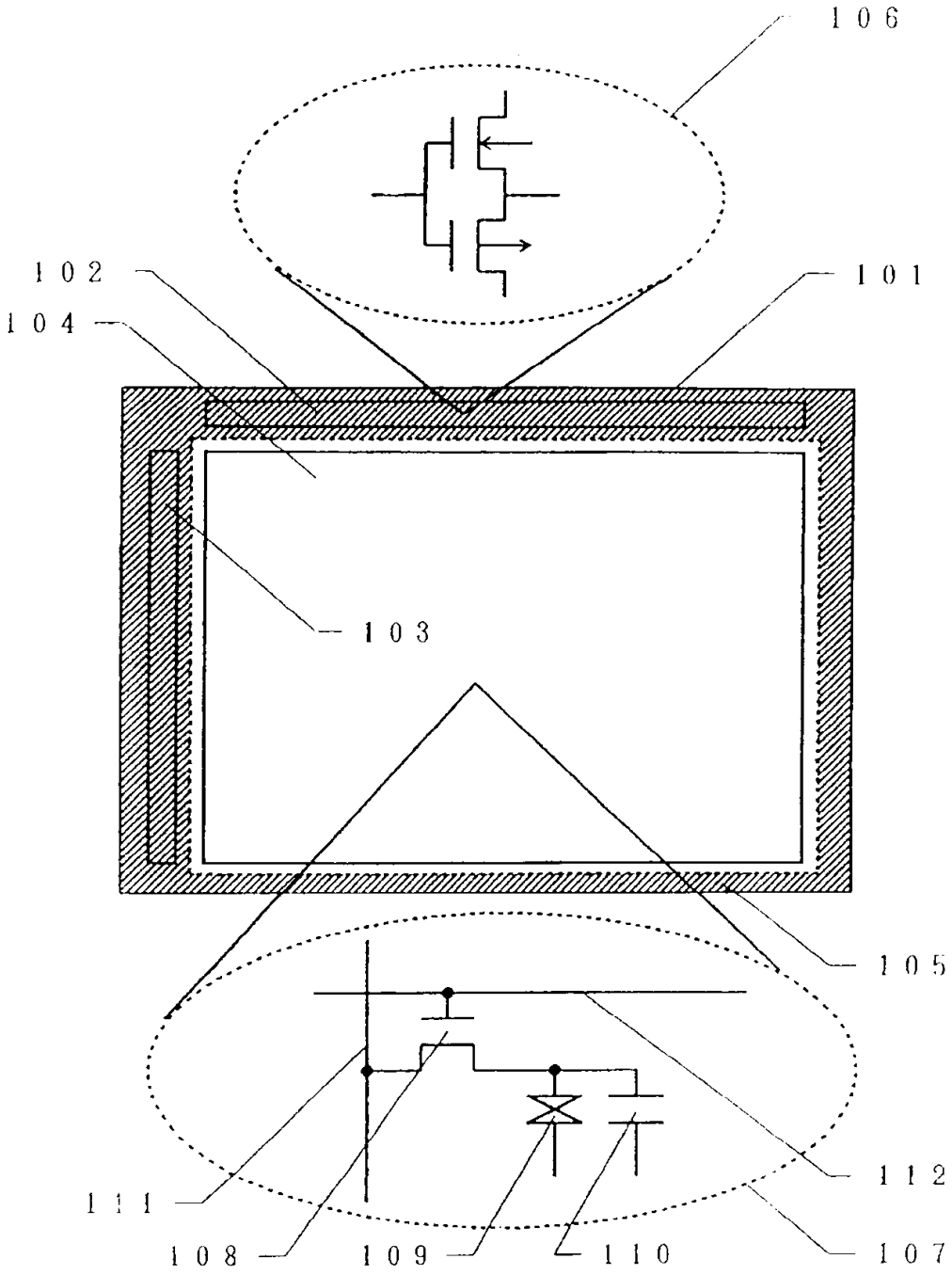
438 SPACER

439 LIQUID CRYSTAL MATERIAL

[REFERENCE NO] P003339－01

[DOCUMENT NAME] DRAWING

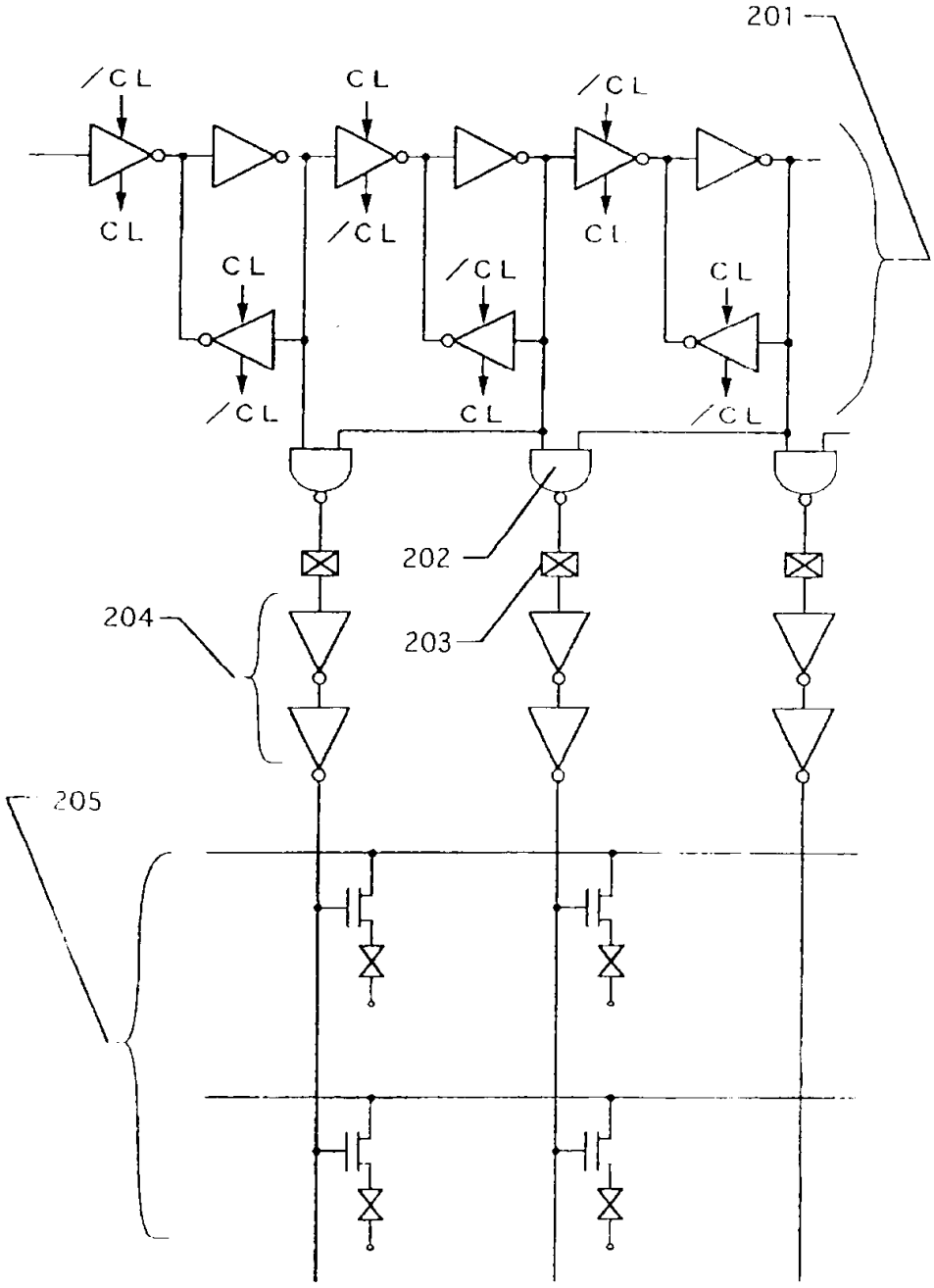
[FIG. 1]



[REFERENCE NO.] P003339 – 01

[FIG. 2]

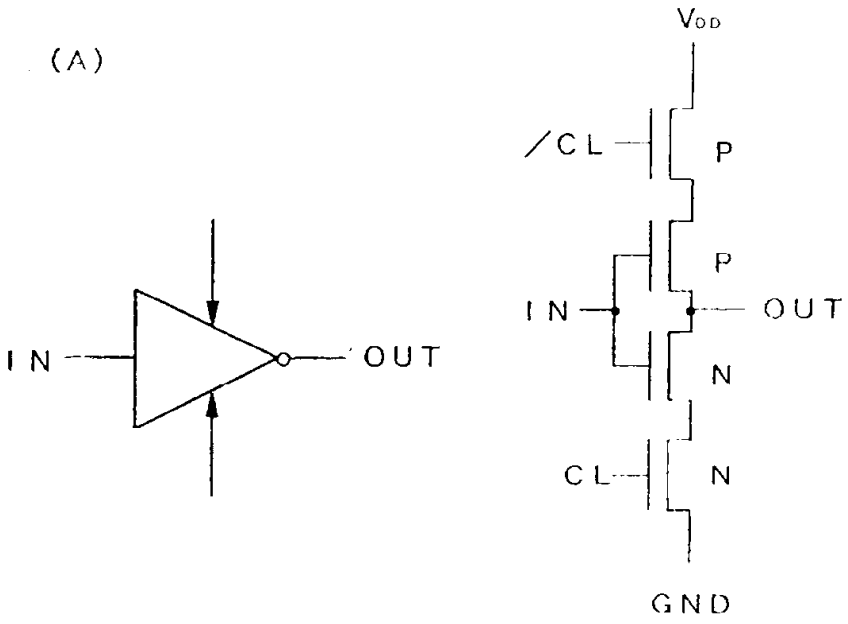
GATE DRIVER CIRCUIT



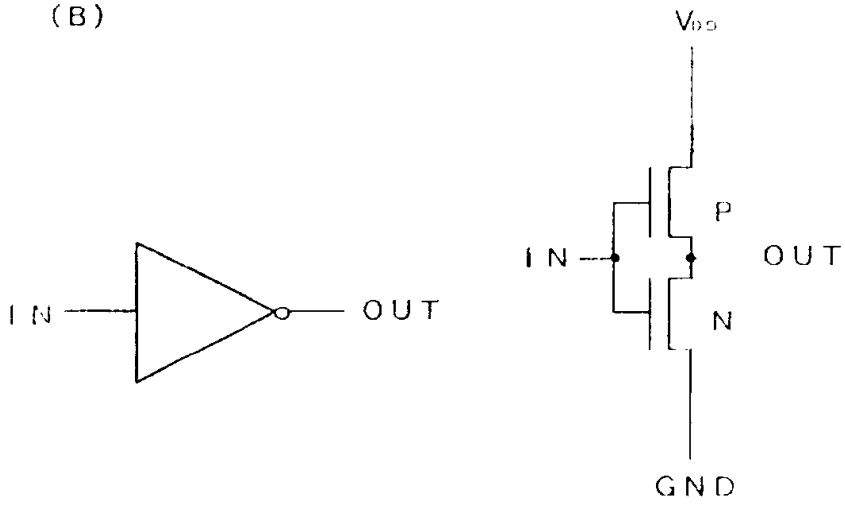
[REFERENCE NO] P003339 – 01

[FIG. 3]

CLOCKED INVERTER

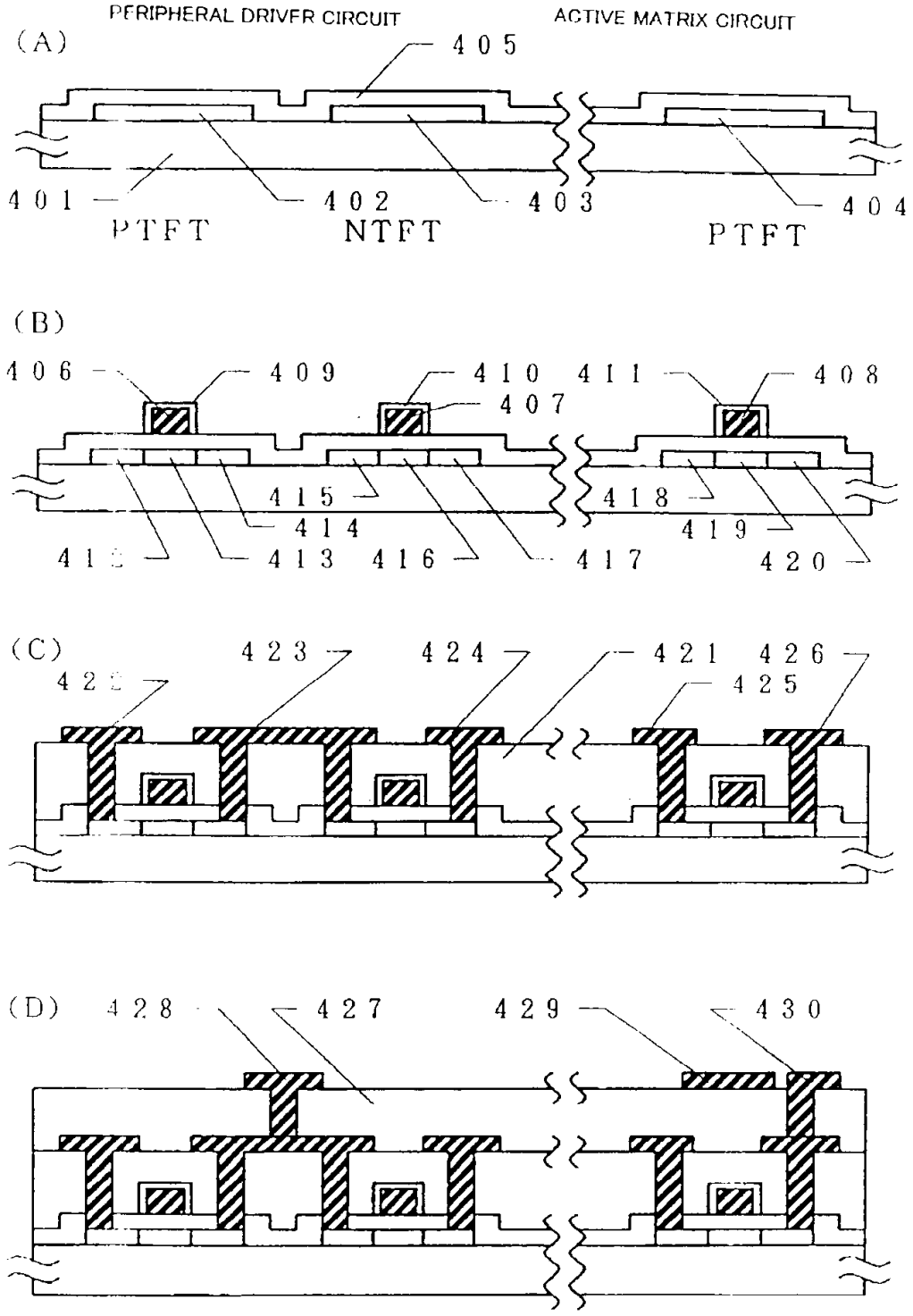


INVERTER



[REFERENCE NO] P003339 −01

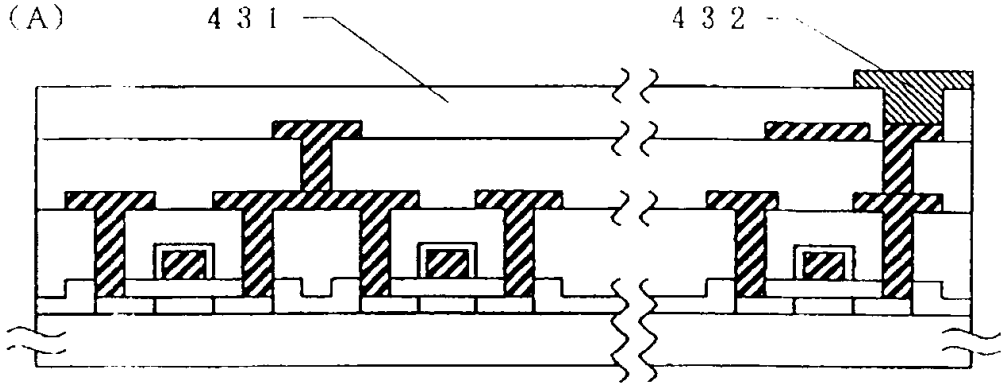
[FIG. 4]



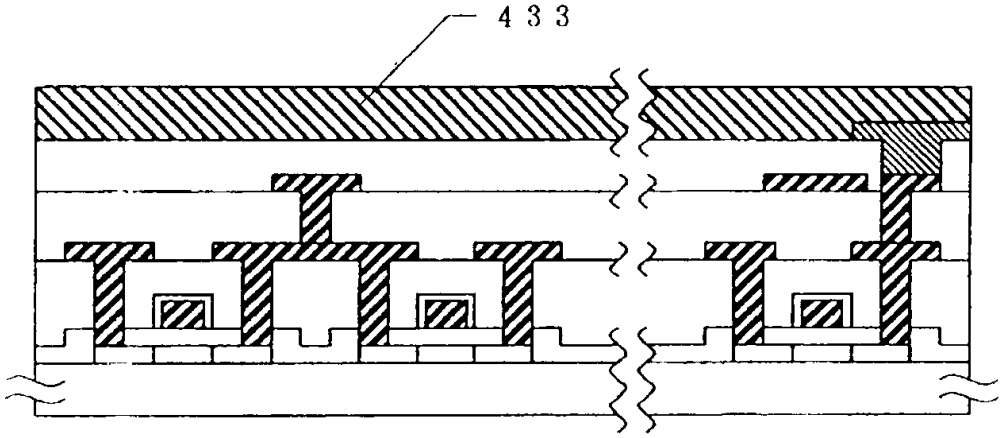
[REFERENCE NO.] P003339 – 01

[FIG. 5]

(A)

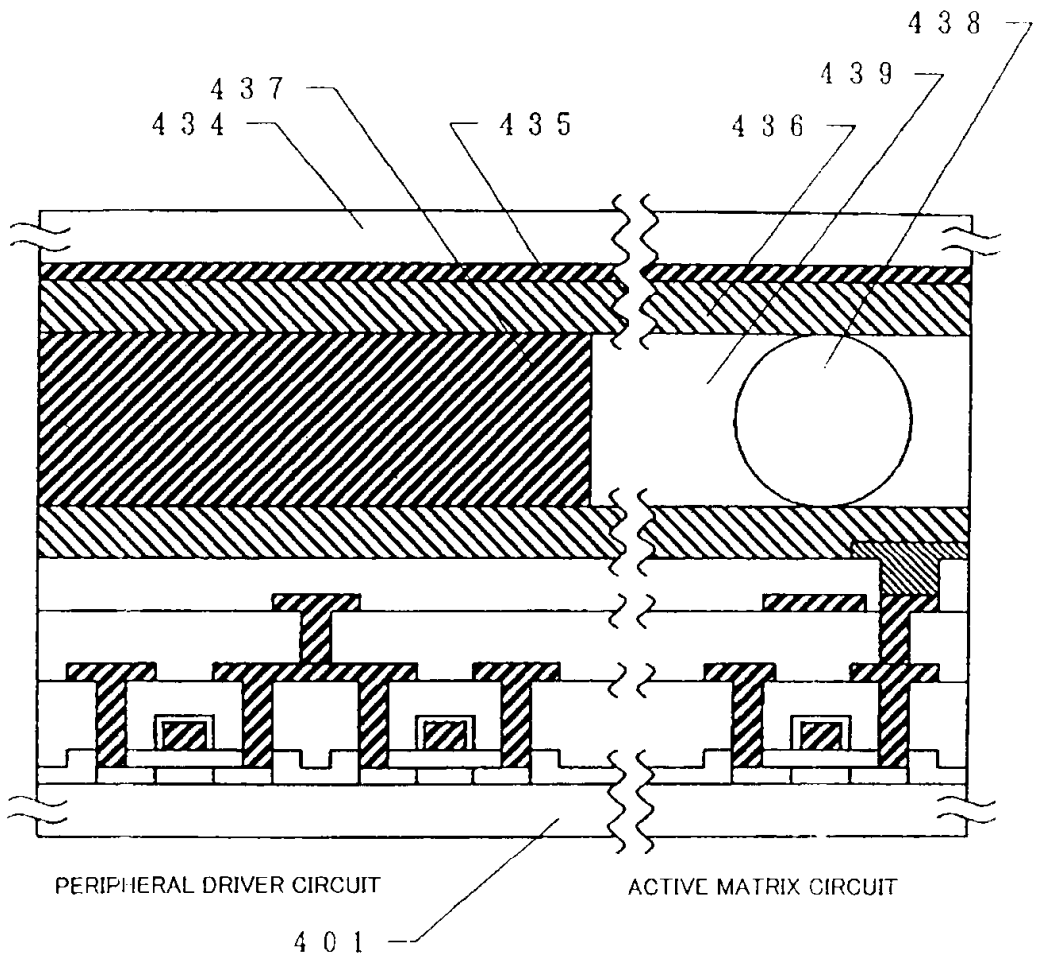


(B)



[REFFRENCE NO.] P003339 – 01

[FIG. 6]



[REFERENCE NO.] P003339 - 01

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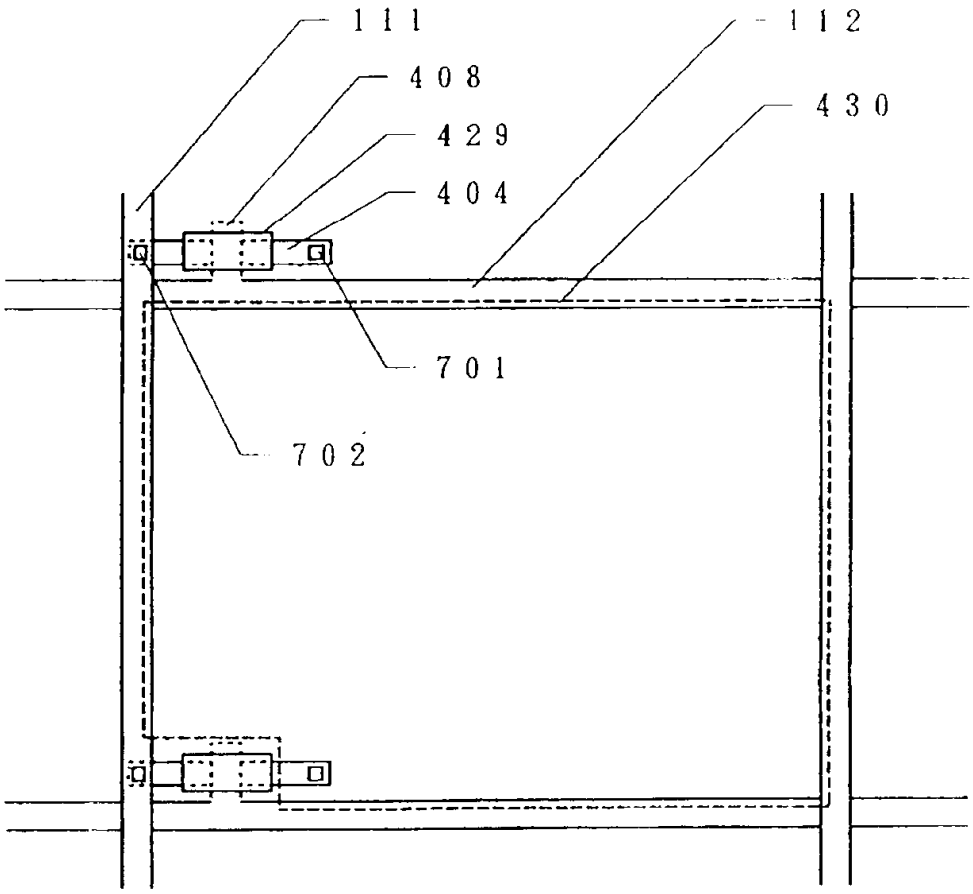
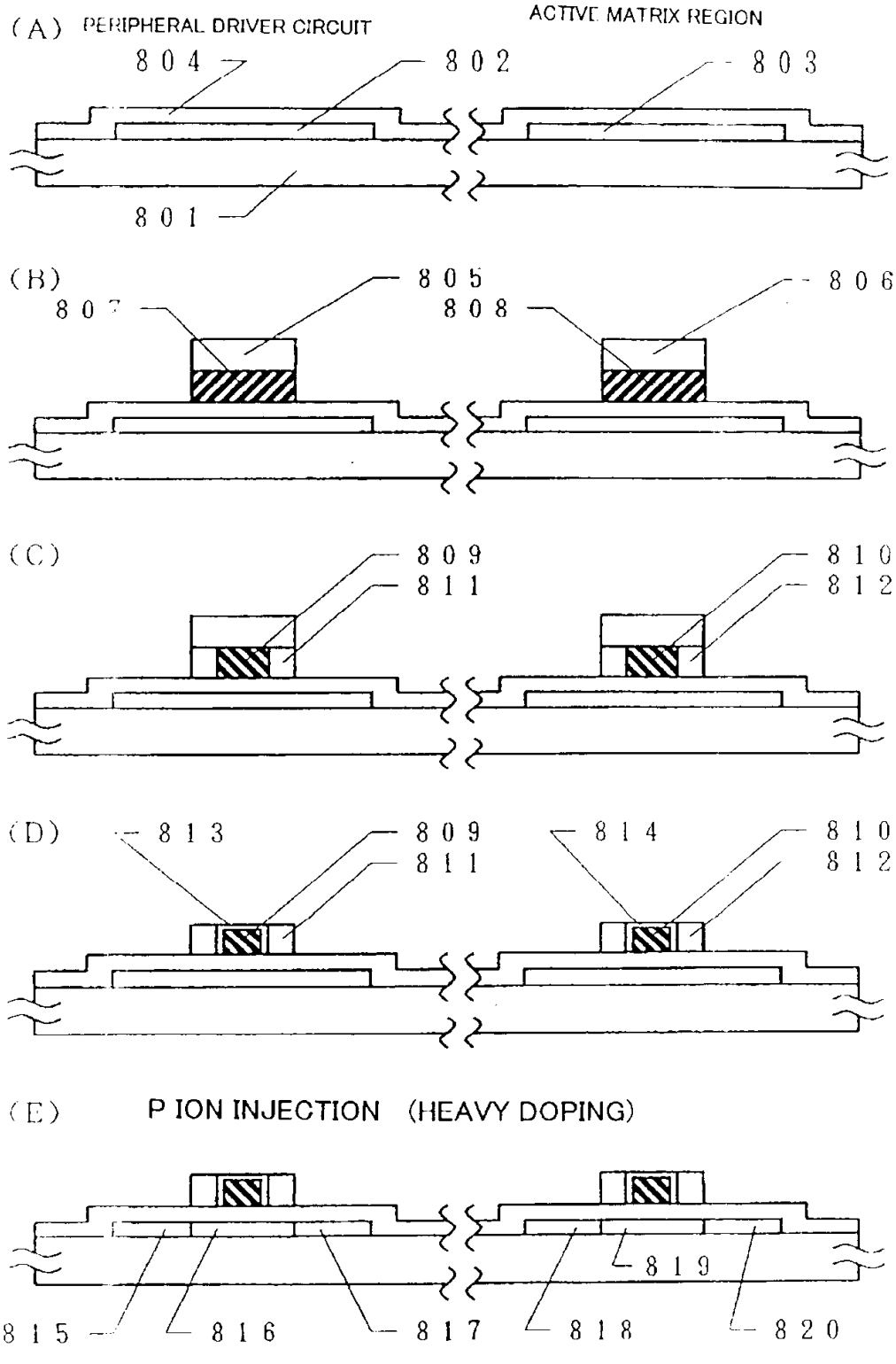
[FIG. 7]



[REFERENCE NO.] P003339 - 01

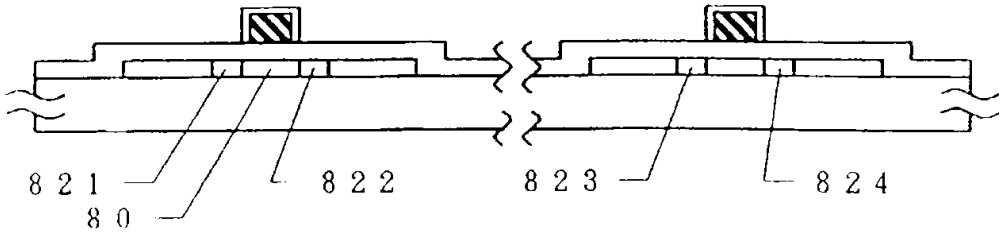
[FIG. 8]



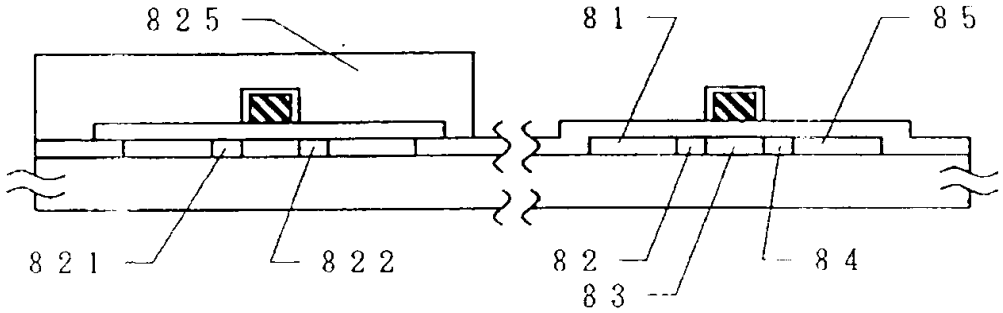
[REFERENCE NO.] P003339 - 01

[FIG. 9]

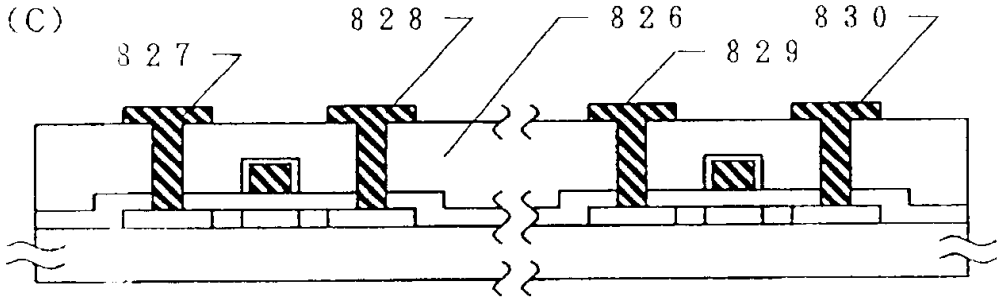
(A) P ION INJECTION (LIGHT DOPING)



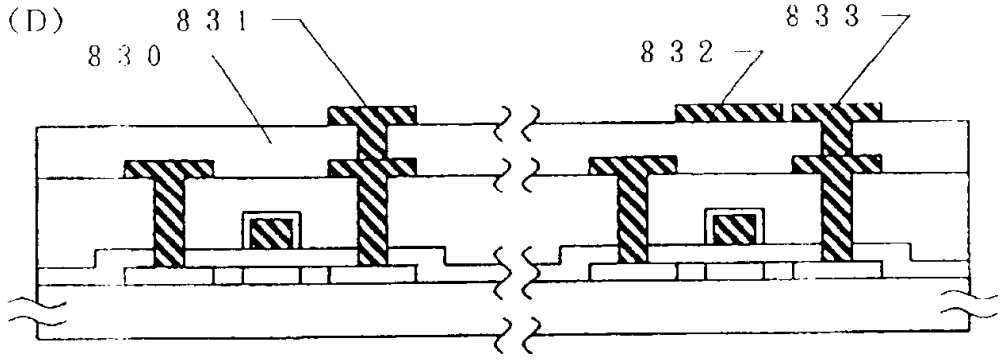
(B) B ION INJECTION



(C)



(D)

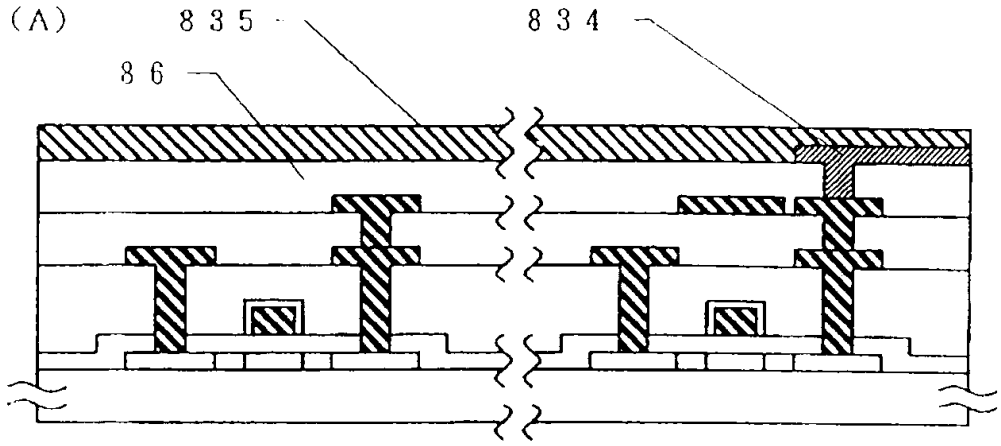


PERIPHERAL DRIVER CIRCUIT ACTIVE MATRIX CIRCUIT

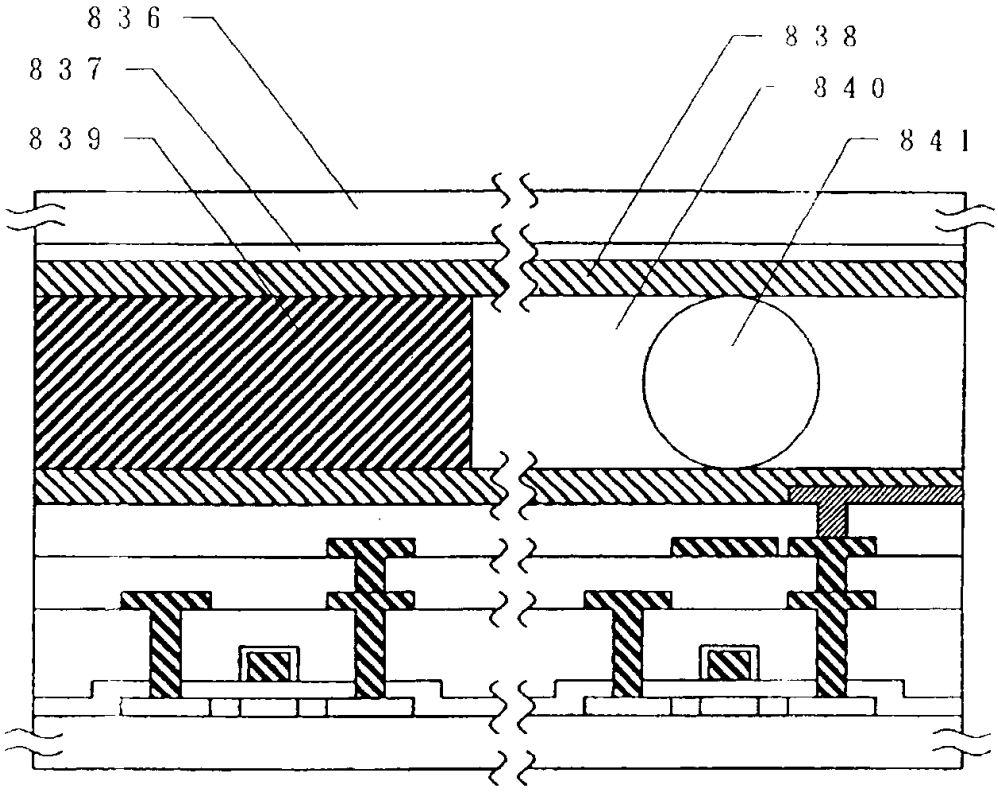
[REFERENCE NO.]P003339 - 01

[FIG. 10]

(A)



(B)



[Name of Document] Abstract

[Summary]

[Problem]

An active matrix liquid crystal display device integrated with a peripheral driver circuit therein is miniaturized in size.

[Structure]

A pair of glass substrates is bonded together and peripheral driver circuits 102 and 103 are disposed in a sealing member 105 in which a liquid crystal material is sealed. That is, the peripheral driver circuits are covered with the sealing member. This structure enables the entire device to be miniaturized in size. Further, by giving a light blocking function to the sealing member, no separate light blocking film is needed.

[Selected Drawing] Fig. 1